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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/721,966 | 11/25/2003 | Timothy W. Budell | END920030108US1 | 5924 |

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| EXAMINER | |
|---|---|
| LE, TOAN M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2863 | |

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/721,966 | BUDELL ET AL. | |
| | Examiner | Art Unit | |
| | Toan M. Le | 2863 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-30* is/are allowed.

6)☒ Claim(s) *1,2,8-14 and 20-23* is/are rejected.

7)☒ Claim(s) *3-7 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

Claim 16 is objected to because of the following informalities:

Claim 16, line 1, "claim 16" should read -claim 13-.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 8-14, and 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by "Survey of Computer-Aided Electrical Analysis of Integrated Circuit Interconnections", Ruehli (referred hereafter Ruehli).

Referring to claim 1, Ruehli discloses an electrical resistance determination method, comprising the steps of

specifying as input to a computer readable program code a description of at least one electrical network comprised by a first substrate, said description including specification of a plurality of first ports on a first side of the first substrate for each electrical network such that all of said first ports are electrically isolated from one another, said description further including specification of a plurality of second ports on a second side of the first substrate for each electrical network such that all of said second ports are electrically connected to a common voltage (figure 1; Abstract; page 627, 2nd col., last paragraph; pages 628-629, section 2); and

executing said computer readable program code by a processor of a computer system, said executing including computing for a first electrical network of the at least one electrical network an electrical resistance between each first port and port of the second ports (page 628, 1st col., last paragraph and 2nd col., 1st paragraph).

As to claim 2, Ruehli discloses an electrical resistance determination method, wherein the electrical resistance is an unadjusted electrical resistance between each first port and the port of the second ports (equations 1 and 3).

Referring to claim 8, Ruehli discloses an electrical resistance determination method, said computing including:

calculating a voltage at each said first port, given an electrical current specified at each said first port; and

computing said electrical resistances from said specified electrical currents and said calculated voltages (equations 1 and 3; page 628, section 2: 1st and 2nd paragraphs).

As to claim 9, Ruehli discloses an electrical resistance determination method, said specifying including:

providing a design of the at least one electrical network comprised by the substrate; and

determining from said design said input to the computer readable-program code (Abstract; figures 1 and 9).

Referring to claim 10, Ruehli discloses an electrical resistance determination method, wherein the first substrate comprises a chip carrier (figure 1).

Referring to claim 11, Ruehli discloses an electrical resistance determination method, further comprising:

specifying as input to the computer readable program code a description of at least one electrical network comprised by a second substrate, said description including specification of a plurality of third ports on a side of the second substrate for each electrical network of the second substrate such that all of said third ports are electrically isolated from one another (figure 1; page 627, 1st col., 3rd paragraph); and

specifying as input to the computer readable program code a description of electrical interconnections between the first ports of the first substrate and the third ports of the second substrate, said computing of each said electrical resistance taking into account said electrical interconnections and said at least one electrical network comprised by said second substrate (page 628, 1st col., last paragraph and 2nd col., 1st paragraph).

As to claim 12, Ruehli discloses an electrical resistance determination method, wherein the first substrate comprises a chip carrier, and wherein the second substrate comprises a semiconductor chip (figure 1).

Referring to claim 13, Ruehli discloses a computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the computer readable program code is adapted to perform an electrical resistance determination by a method comprising the steps of:

receiving input, said input including a description of at least one electrical network comprised by a first substrate, said description including specification of a plurality of first ports on a first side of the first substrate for each electrical network such that all of said first ports are electrically isolated from one another, said description further including specification of a plurality of second ports on a second side of the first substrate for each electrical network such

that all of said second ports are electrically connected to a common voltage (figure 1; Abstract; page 627, 2nd col., last paragraph; pages 628-629, section 2); and

executing said computer readable program code by a processor of a computer system, said executing including computing for a first electrical network of the at least one electrical network an electrical resistance between each first port and a port of the second ports (page 628, 1st col., last paragraph and 2nd col., 1st paragraph).

As to claim 14, Ruehli discloses a computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the computer readable program code is adapted to perform an electrical resistance determination by a method, wherein the electrical resistance is an unadjusted electrical resistance between each first port and the port of the second ports (equations 1 and 3).

Referring to claim 20, Ruehli discloses a computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the computer readable program code is adapted to perform an electrical resistance determination by a method, said computing including:

calculating a voltage at each said first port, given an electrical current specified at each said first port; and

computing said electrical resistances from said specified electrical currents and said calculated voltages (equations 1 and 3; page 628, section 2: 1st and 2nd paragraphs).

As to claim 21, Ruehli discloses a computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the

computer readable program code is adapted to perform an electrical resistance determination by a method, said specifying including:

providing a design of the at least one electrical network comprised by the substrate; and determining from said design said input to the computer readable program code (Abstract; figures 1 and 9).

Referring to claim 22, Ruehli discloses a computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the computer readable program code is adapted to perform an electrical resistance determination by a method, further comprising:

specifying as input to the computer readable program code a description of at least one electrical network comprised by a second substrate, said description including specification of a plurality of third ports on a side of the second substrate for each electrical network of the second substrate such that all of said third ports are electrically isolated from one another (figure 1; page 627, 1st col., 3rd paragraph); and

specifying as input to the computer readable program code a description of electrical connections between the first ports of the first substrate and the third ports of the second substrate, said computing of each said electrical resistance taking into account said electrical interconnections and said at least one electrical network comprised by said second substrate (page 628, 1st col., last paragraph and 2nd col., 1st paragraph).

As to claim 23, Ruehli discloses a computer program product, comprising a computer usable medium having a computer readable program code embodied therein, wherein the computer readable program code is adapted to perform an electrical resistance determination by

a method, wherein the first substrate comprises a chip carrier, and wherein the second substrate comprises a semiconductor chip (figure 1).

Claims 3-7 and 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reason for allowance of the claims 3-4 and 15-16 is the inclusion of a nearest-neighbor adjusted electrical resistance between each first port and the port of the second ports with respect to a second electrical network in accordance with Delaney Triangulation.

The reason for allowance of the claims 5-7 and 17-19 is the inclusion of displaying a perspective plot of electrical resistances numerically as a bar oriented about normal to each first port on the first side of the substrate having a height that is a monotonically increasing function linearly at the first port at which the bar is located, also having a color or shade of gray that is reflective of a range of electrical resistances.

***Allowable Subject Matter***

Claims 24-30 are allowed.

The reason for allowance of the claims 24-26 and 29 is the inclusion of the steps of specifying a description of N electrical networks comprised by a first substrate including specification of a plurality of first ports on a first side of the substrate for each electrical network electrically isolated from one another and specification of a plurality of second ports on a second side of the substrate for each electrical network electrically connected to a common voltage and computing for each electrical network the N electrical networks an unadjusted electrical

resistance between each first port and a port of the second ports collectively satisfying acceptance criteria.

The reason for allowance of the claims 27-28 is the inclusion of the step of displaying a perspective plot of electrical resistances numerically as a bar oriented about normal to each first port on the first side of the substrate having a height that is a monotonically increasing function linearly at the first port at which the bar is located, also having a color or shade of gray that is reflective of a range of electrical resistances.

The reason for allowance of the claim 30 is the inclusion of the electrical network comprised by a second substrate including specification of a plurality of third ports on a side of the second substrate for each electrical network electrically isolated from one another and specification of electrical interconnections between the first ports of the first substrate and the third ports of the second substrate in computing an unadjusted electrical resistance of that electrical interconnections.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Transient and Crosstalk Analysis of Interconnection Lines for Single Level Integrated Packaging Modules", Zheng et al., 1998 IEEE, Pages 120-123

"Substrate Modeling and Lumped Substrate Resistance Extraction for CMOS ESD/Latchup Circuit Simulation", Li et al., 1999 ACM, Pages 549-554

"Modeling and Characterization of the Polymer Stud Grid Array (PSGA) Package: Electrical, Thermal and Thermo-Mechanical Qualification", Chandrasekhar et al., 2001 Electronic Components and Technology Conference

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

April 28, 2005

John Barlow
Supervisory Patent Examiner
Technology Center 2800